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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification <sup>6</sup> : <b>H01J 29/70</b>	A1	(11) International Publication Number: <b>WO 99/03126</b>
		(43) International Publication Date: 21 January 1999 (21.01.99)

(21) International Application Number: PCT/US98/13802	(81) Designated States: CA, CN, IL, JP, KR, RU, SG, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).
(22) International Filing Date: 2 July 1998 (02.07.98)	

(30) Priority Data:  
60/052,228 11 July 1997 (11.07.97) US  
09/073,342 6 May 1998 (06.05.98) US

**Published**  
With international search report.  
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

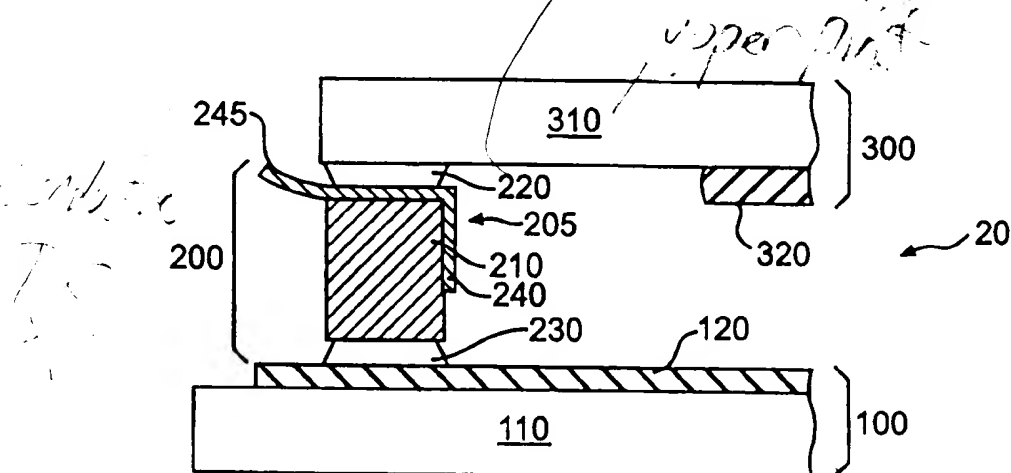
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*modification seating  
material*

(54) Title: FLASHOVER CONTROLLING SPACER FOR PARALLEL PLATE ELECTRON BEAM DEVICE



(57) Abstract

A structure to reduce the likelihood of flashover in a parallel plate electron beam array is disclosed. The structure may comprise a means for generating a low intensity electric field in the vicinity of a spacer (200) separating the parallel plates of the array (100), and the anode (300). The presence of the electric field in the vicinity of the spacer is not conducive to the occurrence of a surface supported flashover on the gates and emitters. The electric field means may be provided by a conductive coating (240) on one or more surfaces of the spacer. Alternatively, the electric field means may be provided by a conductive coating on a guard ring located within the array in the vicinity of the spacer. Methods of making the structure are also disclosed.

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to the control of flashover, however, the provision of such insulator layers does not completely solve the flashover problem, and also cannot be provided at zero cost.

In still another approach, which is particularly applicable to large screen FED's, Nakayama *et al.* disclose an FED having a cathode panel and a back panel with space therebetween in U.S. Patent No. 5,223,766, Nakayama *et al.* (June 29, 1993) for an Image Display Device with Cathode Panel and Gas Absorbing Getters. In Nakayama, through holes may be provided in the cathode panel, and the space between the cathode and back panels may be used for containing getters. The inventors in Nakayama state that it is an object of the invention to provide a display device capable of containing a sufficient amount of getter for maintaining a required pressure, wherein the image quality can be maintained at the center of a display screen so that a superior image quality is attainable, even on a large-sized screen. Therefore, in Nakayama, additional getter is provided in the FED so that the pressure within the FED may be higher than it would otherwise have to be to minimize flashover. The increased residual gas pressure, that is acceptable to Nakayama *et al.*, may result in unacceptable levels of flashover despite the additional getter material used.

The problems associated with sidewall induced flashovers, discussed above, may also arise in the interior portions of large sized screen FED's when low internal device pressure is maintained. Internal spacers are commonly used to maintain low (vacuum) pressure within an FED. Internal spacers prevent the FED screen from bowing inward as a result of the vacuum conditions of the FED interior. While the spacers beneficially keep the screen from bowing or breaking, the spacers also provide a surface linking the gate and anode which can facilitate flashovers.

Accordingly, there is a need for new methods and apparatus for reducing the occurrence of flashover, without reducing the level of anode voltages. There is also a need for methods and apparatus for reducing the magnitude of damage suffered from the occurrence of flashovers during the initial burn-in and operation of the device. There is a particular need for a device which does not support surface flashovers along the interior surfaces and/or internal spacers of the device. The present invention meets this need, and provides other benefits as well.

### **Objects of the Invention**

It is therefore an object of the present invention to provide methods and apparatus for reducing the occurrence of flashovers in parallel plate electron beam arrays.

It is another object of the present invention to provide methods and apparatus for reducing the amount of damage suffered from the occurrence of flashovers in parallel plate electron beam arrays.

It is a further object of the present invention to provide methods and apparatus for reducing the occurrence of flashovers which are supported by spacers in parallel plate electron beam arrays.

It is yet another object of the present invention to provide a means for providing a low intensity electric field in the vicinity of a spacer in a parallel plate electron beam array.

It is still yet another object of the present invention to provide methods and apparatus for increasing anode voltages in a parallel plate electron beam array without increasing the occurrence of flashovers in the array.

It is still a further object of the present invention to provide methods and apparatus for reducing the occurrence of flashovers in parallel plate electron beam arrays by absorbing residual gas therein.

Additional objects and advantages of the invention are set forth, in part, in the description which follows and, in part, will be apparent to one of ordinary skill in the art from the description and/or from the practice of the invention.

### **Summary of the Invention**

In response to the foregoing challenge, Applicants have developed an innovative, economical electron beam array device comprising: a lower plate and an upper plate connected along an outer perimeter by a continuous spacer structure; and means for providing a low intensity electric field region along at least one surface of said spacer structure.

Applicants have also developed an innovative and economical method of making an electron beam array device comprising the steps of: providing a lower plate, an upper

plate, and a glass plate; removing a selective portion of said glass plate to form a glass frame; providing a conductive coating on a surface of said glass frame; and sealing said glass frame between said lower plate and said upper plate.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only, and are not restrictive of the invention as claimed. The accompanying drawings, which are incorporated herein by reference, and which constitute a part of this specification, illustrate certain embodiments of the invention, and together with the detailed description serve to explain the principles of the present invention.

### **Brief Description of the Drawings**

Fig. 1 is a cross-sectional view in elevation of a known type of electron beam array device.

Fig. 2 is a cross-sectional view in elevation of the edge region of a first electron beam array embodiment of the invention.

Figs. 3A, 3B, and 3C are alternative embodiments of the spacer structure shown in Fig. 2.

Fig. 4 is a plan view of an exemplary insulator frame employed in the invention.

Fig. 5 is a cross-sectional view in elevation of the edge region of a second electron beam array embodiment of the invention.

Fig. 6 is a combined cross-sectional view in elevation and pictorial view of the device shown in Fig. 5.

Fig. 7 is a cross-sectional view in elevation of a third electron beam array embodiment of the invention.

Fig. 8 is a cross-sectional view in elevation of a fourth electron beam array embodiment of the invention.

### **Detailed Description of the Preferred Embodiments**

Reference will now be made in detail to a preferred embodiment of the present invention, an example of which is illustrated in the accompanying drawings. A preferred

embodiment of the present invention is shown in Fig. 2 as the edge portion of device 20. Device 20 may be any parallel plate electron beam array, including a field emitter display.

Device 20 comprises a lower plate 100, an upper plate 300, and a spacer structure 200. The spacer structure 200 includes a means for providing a low intensity electric field 205 along at least one surface of the spacer structure. The electric field means 205 may comprise a conductive coating 240, of material such as chromium, nickel, gold, silver platinum, chromium oxide, amorphous diamond, or diamond like films on a surface of an insulator frame or ring 210. The presence of the conductive coating 240 may generate a low intensity electric field in the vicinity of the insulator frame 210. This electric field region does not readily support an electron flashover over the surface of the insulator frame 210. When the conductive coating is maintained at a certain potential (typically zero) there exists a field between the anode 320 and the conductive coating 240. As described earlier, the residual gas molecules released as a result of electron bombardment of phosphor will immediately tend to flow towards the perimeter of the device. Before the equilibrium pressure is reached, there is likelihood of the build-up of local pressure at the regions of the sidewall (i.e., spacer and frit). In the absence of the coating 240, the electric field existing between the anode 320 and one of the elements of plate 100 will cause a gas discharge breakdown flashover) if the pressure and the spacing between the anode and one of the elements of plate 100, are appropriate for a pachen breakdown criterion. This breakdown will ruin the gate and emitter elements of plate 100. This destructive flashover can be prevented if there is an electric field between the anode and conductive coating 240. This field will take over the breakdown of the gas and thus prevent the flashover on the vital elements of plate 100. The coating 240 and its potential close to zero acts similar to the "lightning arrester" of a building.

In a preferred embodiment of the invention, device 20 may be constructed in the following manner. The insulator frame 210 (or guard ring 250 in Fig. 5 discussed below) may first be formed from a sheet of insulative material, such as glass. The frame 210 may be formed by trimming the glass sheet so that the outer dimension of the glass sheet is approximately the same as the outer dimension of the upper plate 300. With reference

forming sidewall ridges to support the corrugated structure by etching or molding. Alternatively, a similarly profiled structure could be formed by stacking alternating layers of insulators and conductors (e.g. glass for insulators and nickel foil for conductors).

Following the deposit of the conductive coating 240 on the frame 210, a layer of insulative sealing material 230, such as frit glass, a ceramic frit, or a meltable glass rod, may be applied to the lower plate 100. The frit glass 230 protects and insulates the conductor element 120 from contact with the conductive coating 240. The frit glass 230 also seals the frame 210 to the lower plate 100. Next, a layer of insulating sealing material 220 may be applied to the upper surface of the frame 210, or the lower surface of the upper plate 310, and the upper plate-spacer structure-lower plate sandwich may be pressed together to form the device 20. The completed device 20 is sealed along its periphery such that the interior of the device may be evacuated and maintained in vacuum.

In a preferred embodiment of the invention, one or more of the foregoing steps may be carried out in an evacuated chamber, or in an inert atmosphere. By constructing the device 20 in a vacuum or inert atmosphere, the oxidation of the conductive coating 240 may be reduced, thereby enhancing the electric field generating capability of the conductive coating.

With reference to Fig. 5, in which like reference numerals refer to like elements shown in the other figures, an alternative embodiment of the invention is shown. In the embodiment shown in Fig. 5 the electric field means 205 may not be provided by an insulator frame with a conductive coating. Instead, the electric field means 205 may be provided by an insulating guard ring 250 having a conductive coating 260. The insulating guard ring 250 and conductive coating 260 may be constructed in accordance with the foregoing explanation of the construction of the insulator frame 210 and the conductive coating 240.

After the conductive coating 260 is deposited on the guard ring 250, the guard ring may be connected to the lower plate 100 with a layer of insulative sealing material 230. The conductive coating 260 may be provided with a conductive tab 270 which connects the coating 260 with an externally applied electric potential. In the same

manner, with reference to Fig. 2, the conductive coating 240 on the spacer may be provided with a conductive tab 245 connecting the coating 260 to an electric potential.

The guard ring 250 may have an outer dimension which is smaller than that of the insulator frame 210. Thus, in order to connect both the guard ring 250 and the insulator frame 210 to the lower plate 100 with the sealing material 230, the sealing material must extend into the interior of the device 20 sufficiently that it is wide enough to accommodate both the insulator frame and the guard ring.

With continued reference to Fig. 5, the guard ring 250 with the conductive coating 260 provides a low intensity electric field in the vicinity of the edge portion of the device 20. The presence of this electric field reduces the likelihood of the occurrence of flashovers in the edge portion of the device. Fig. 6, in which like numerals refer to like elements shown in the other figures, shows a combined cross-sectional and pictorial view of the device 20 of Fig. 5.

A third electron beam array embodiment of invention is shown in Fig. 7, in which like reference numerals refer to like elements shown in the other figures. The embodiment of Fig. 7 modifies the previously described embodiments of the invention by adding a space 410 below the lower plate 100 for the placement of getter material.

In Fig. 7, the lower plate 100 is sealed to a back plate 400 along the outer periphery of the lower and back plates. The lower plate 100 and back plate 400 may be sealed with a spacer structure 500 which is similar in design to the above described spacer structure 200. The lower plate 100 is sealed to the back plate 400 such that a space 410 is formed between the two plates. The seal between the plates may have sufficient integrity to permit a vacuum to be maintained in the space 410.

The undersurface of the lower plate may be coated with a layer of getter material 140. The upper surface of the back plate 400 may also be coated with a layer of getter material 420. The lower plate 100 may be provided with one or more through holes 130 which facilitate the migration of gas molecules between the space above the lower plate 100 and the space 410 below the lower plate 100. In this manner, gas molecules



outgassed in the space above the lower plate 100 may migrate to and be captured by the layers of getter material 140 and 420.

The back plate 400 may be constructed of glass or another suitable support material. The back plate 400 may be sufficiently thick as to bear much, if not all, of the ambient pressure on the bottom of the device resulting from the interior of the device 20 being a vacuum. The upper plate 310 may also be sufficiently thick as to bear much, if not all, of the ambient pressure on the top of the device 20. In order for the upper plate 310 to bear all of the pressure on the top of the device 20, the upper plate 310 should be dimensioned such that the spacer structure 200 is substantially directly overlying the spacer structure 500. In this manner the lower plate 100 may be shielded from having to bear significant pressure forces, and accordingly may be made of thinner material than it otherwise might. With the use of a thick upper plate 310 and a thick back plate 400, large screen (25 to 40 inch diagonal) devices 20 may be constructed without the use of internal spacers in the devices.

A fourth electron beam array embodiment of invention is shown in Fig. 8, in which like reference numerals refer to like elements shown in the other figures. The embodiment shown in Fig. 8 is similar to that of Fig. 7, with the exception of the addition of a cover plate 600 and a thinner upper plate 310. In the Fig. 8 embodiment, a thick cover plate 600 of glass or other suitable material may be used to bear much, if not all, of the pressure on the top of the device 20. The cover plate 600 may be sealed to the upper plate 310 about the respective peripheries of the plates with a spacer structure 500. The upper plate 310 may be thinner than it otherwise might be because it is not required to withstand much, if any, of the pressure on the top or bottom of the device 20. The upper plate 310 may be provided with one or more through holes 330 which permit equalization of the vacuum condition in the interior spaces above and below the upper plate 310.

It will be apparent to those skilled in the art that various modifications and variations can be made in the construction, configuration, and/or operation of the present invention without departing from the scope or spirit of the invention. For example, in the embodiments mentioned above, various changes may be made to the sealing materials

used to connect the insulator frame with the upper and lower plates of the device. Further, changes may be made to the order in which the upper and lower plates are sealed to the insulator frame, and to which of the elements (the frame or the plates) the sealing means is first applied. Changes may also be made to the shape, size, and wall width of the insulator frame (or guard ring) without departing from the scope or spirit of the invention. Further, it may be appropriate to make additional modifications or changes to the location of the conductive coating on the insulator frame in order to vary the effect and strength of the electric field means on a device by device basis. Thus, it is intended that the present invention cover the modifications and variations of the invention provided they come within the scope of the appended claims and their equivalents.

## WE CLAIM:

1. An electron beam array device comprising:  
a lower plate and an upper plate connected along an outer perimeter by a continuous spacer structure; and  
means for providing a low intensity electric field region along at least one surface of said spacer structure.
2. The device of Claim 1 wherein said electric field means comprises a coating of conductive material on a surface of said spacer structure.
3. The device of Claim 1 wherein said coating comprises a material selected from the group consisting of: chromium, nickel, gold, silver, platinum, chromium oxide, amorphous diamond, or diamond like films.
4. The device of Claim 1 wherein said spacer structure comprises an insulator frame and said electric field means is provided on an outer surface of said insulator frame.
5. The device of Claim 4 wherein said insulator frame comprises a material selected from the group consisting of: glass and ceramic.
6. The device of Claim 1 wherein said spacer structure comprises an insulator frame and a guard ring within said insulator frame, and wherein said electric field means is provided on an outer surface of said guard ring.
7. The device of Claim 6 wherein said guard ring comprises a material selected from the group consisting of: glass and ceramic.
8. The device of Claim 1 wherein said low intensity electric field has an intensity in the range of 100V/mm to 10,000V/mm.
9. The device of Claim 1 further comprising a back plate connected to the lower plate along an outer perimeter of an under surface of the lower plate, said back plate having a through hole therein providing communication between a space above the lower plate and a space below the lower plate;  
wherein a layer of getter material is provided in said space below said lower plate.

10. The device of Claim 9 wherein said layer of getter material is provided on the undersurface of the lower plate.

11. The device of Claim 9 wherein said layer of getter material is provided on an upper surface of the back plate.

12. The device of Claim 9 further comprising a cover plate connected to the upper plate along an outer perimeter of an upper surface of the upper plate, said upper plate having a through hole therein providing communication between a space above the upper plate and a space below the upper plate.

13. The device of Claim 12 wherein said back plate and said cover plate are sufficiently thick as to bear much of the ambient pressure on the top and bottom of the device.

14. In an electron beam array device having a lower plate and an upper plate connected about outer regions thereof by a spacer structure, the improvement comprising:  
a coating of conductive material provided on a portion of said spacer structure, said coating providing an electric field region which reduces the likelihood of a spacer structure supported flashover between the upper and lower plates.

15. A field emitter display comprising:  
an upper plate having an anode associated therewith;  
a lower plate having an array of field emitters and gates associated therewith;  
a spacer structure sealing said upper plate to said lower plate along outer perimeters thereof, said spacer structure comprising a insulator frame, a conductive coating on an upper surface of said insulator frame, an upper glass frit connecting said insulator frame to said upper plate, and a lower glass frit connecting said insulator frame to said lower plate.

16. The field emitter display of Claim 15 further comprising a conductive coating on a side surface of said insulator frame and means to externally apply electric potential to the said conductive coating.

17. The field emitter display of Claim 15 wherein said conductive coating has thickness is in the range of 30 nanometer to 25 microns.

18. The field emitter display of Claim 15 wherein said conductive coating comprises a pointed feature extending from said coating.

19. The field emitter display of Claim 15 further comprising a back plate sealed to and spaced from an under surface of said lower plate, said back plate having an opening therethrough connecting spaces above and below said lower plate . . .

means for absorbing residual gas in said display, said means for absorbing being provided in the space below said lower plate.

20. The field emitter display of Claim 19 further comprising a cover plate sealed to and spaced from an upper surface of said upper plate, wherein said cover plate and said back plate comprise means for insulating said upper plate and lower plate from application of ambient air pressure on the upper and lower surfaces.

21. A field emitter display comprising:

an upper plate having an anode associated therewith;

a lower plate having an array of field emitters and gates associated therewith;

a spacer structure sealing said upper plate to said lower plate along outer perimeters thereof, said spacer structure comprising:

a insulator frame;

an upper glass frit connecting said insulator frame to said upper plate;

a lower glass frit connecting said insulator frame to said lower plate and

having an extension extending into an interior region of said display;

a guard ring provided on said lower glass frit extension; and

means for providing a low intensity electric field on said guard ring.

22. The field emitter display of Claim 21 wherein said electric field means comprises a conductive coating on a surface of said guard ring and means for externally applying electric potential to the said conductive coating.

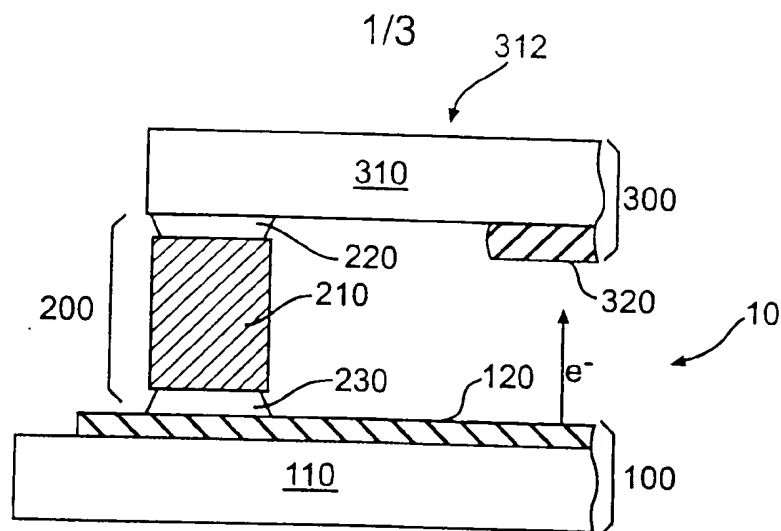
23. The field emitter display of Claim 22 wherein said conductive coating comprises a coating of chromium in the range of 1000 to 2000 angstroms thick.

24. A method of making an electron beam array device comprising the steps of: providing a lower plate, an upper plate, and a glass frame;

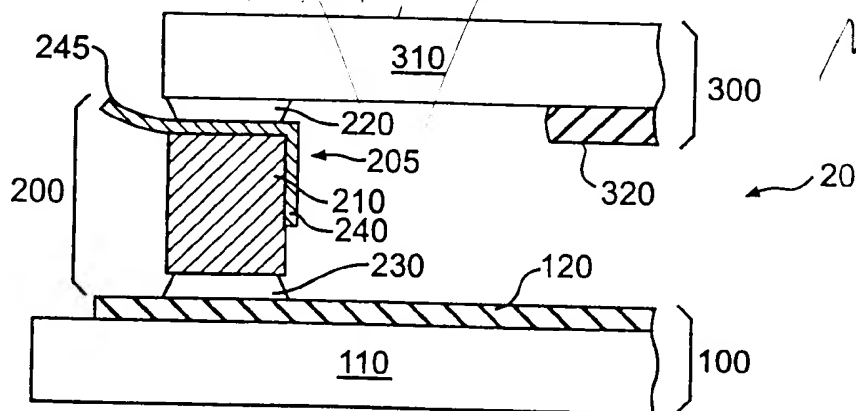
providing a conductive coating on a surface of said glass frame; and

sealing said glass frame between said lower plate and said upper plate.

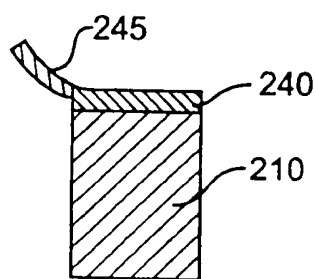
25. The method of Claim 24 wherein the step of providing a conductive coating comprises the step of sputter coating a thin coating of material selected from the group consisting of: chromium, nickel, silver, gold, chromium oxide, amorphous diamond, or diamond like films.



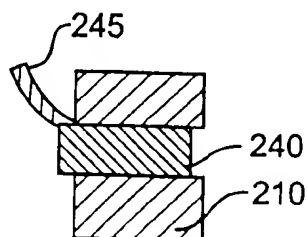
**FIG. 1**  
(PRIOR ART)



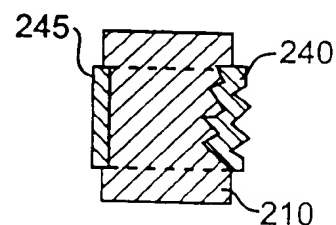
**FIG. 2**



**FIG. 3A**

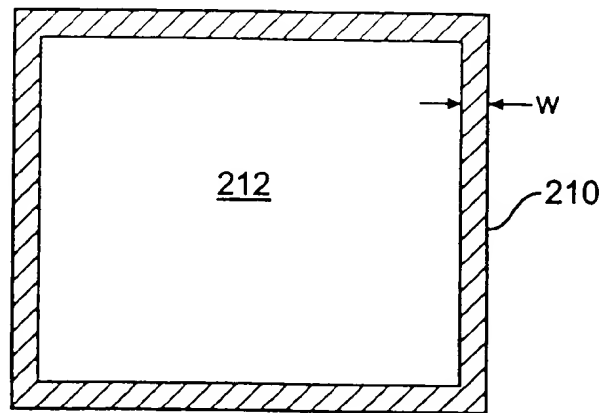
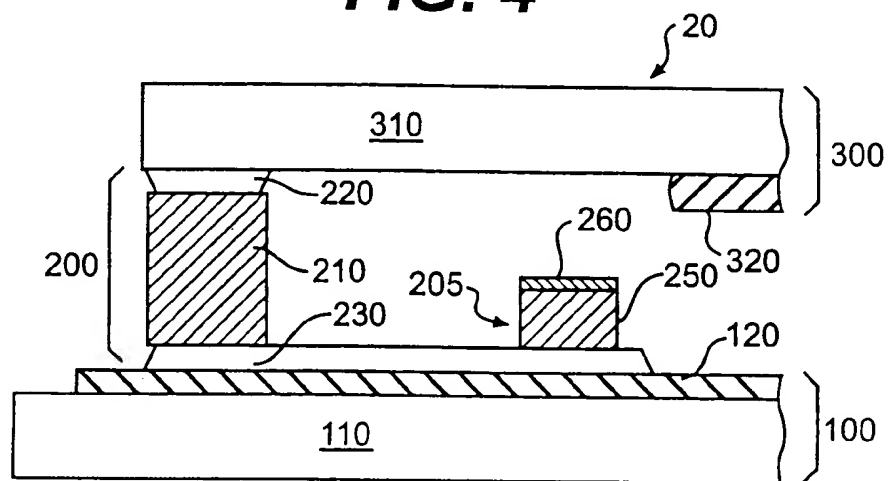
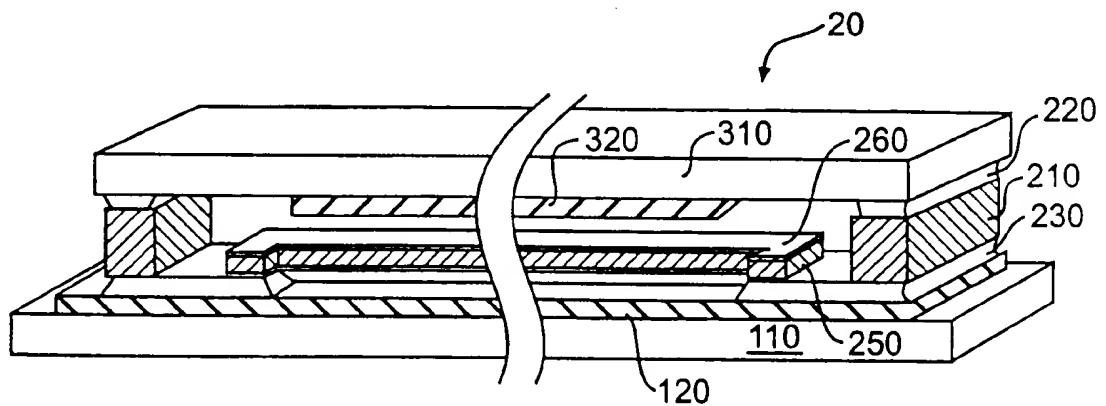


**FIG. 3B**



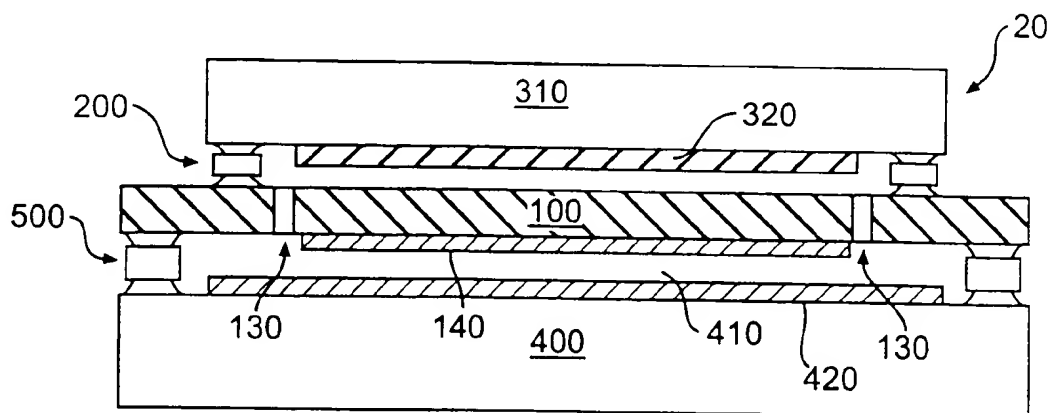
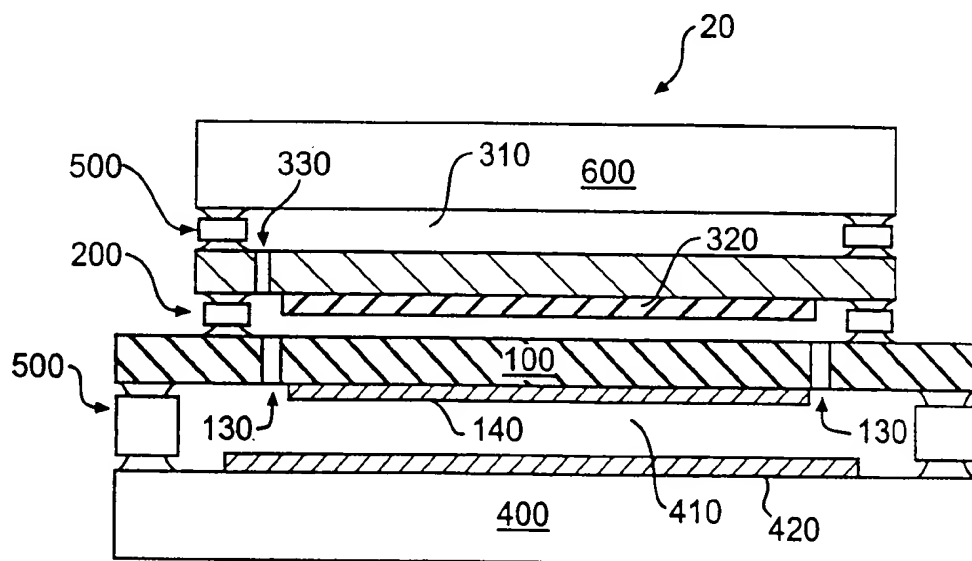
**FIG. 3C**

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**FIG. 4****FIG. 5****FIG. 6**



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**FIG. 7****FIG. 8**

## INTERNATIONAL SEARCH REPORT

International application No  
PCT/US98/13802

<b>A. CLASSIFICATION OF SUBJECT MATTER</b> IPC(6) : H01J 29/70 US CL : 313/495 According to International Patent Classification (IPC) or to both national classification and IPC		
<b>B. FIELDS SEARCHED</b> Minimum documentation searched (classification system followed by classification symbols) U.S. : 313/495, 496, 497, 422 Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched NONE Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) NONE		
<b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A,E	US 5,811,919 A (HOOGSTEEN et al) 22 September 1998 (22.09.98), see the entire document.	1-25
A,P	US 5,770,918 A (KAWATE et al) 23 June 1998 (23.06.98), see the entire document.	1-25
A	US 5,223,766 A (NAKAYAMA et al) 29 June 1993 (29.06.93), see the entire document.	1-25
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